REMARKS

This is a response to the Office Action dated April 10, 2003. Claims 11 and 16 have been amended. Upon entry of the Preliminary Amendment dated March 18, 2003, and the present amendment, claims 11-16 will be pending in the present application.

THE PRELIMINARY AMENDMENT FILED MARCH 18, 2003

Since there was no indication in the Office Action dated April 10, 2003 (hereinafter "the Office Action), that the Examiner had received and entered the preliminary amendment dated March 18, 2003, filed concurrently with the Request for Continued Examination (RCE) as the submission required under 37 C.F.R. §114, the Examiner is requested to confirm that this preliminary amendment was in fact received and entered in the present application. It is noted, for example, that the Preliminary Amendment added a new claim to the present application but that the Examiner did not mention the existence of the new claim in the Office Action.

Upon review of the Preliminary Amendment dated March 18, 2003, the applicant noted that proposed new claim 12 should have been numbered as claim 16 since claims 12-15 were already pending in the present application at the time of filing of the Preliminary Amendment. Accordingly, by this amendment, the applicant has requested that proposed new claim 12 added by the Preliminary Amendment dated March 18, 2003, be renumbered as new claim 16.

In addition, the applicant noted some minor typographical errors in the proposed new claim and has corrected these minor errors by the present amendment. Specifically, the word, "silicone" was replaced by "silicon" to render the claim terminology consistent, the underlining in the claim was deleted, the transitional word, "wherein" was added in the last line of the claim, and the word "insulating" in the last line of the claim was replaced by "insulated" to render the claim terminology consistent. Finally, this claim has also been amended to more specifically require that the third insulating layer must be located directly on the tunnel oxide layer, the select gate and the floating gate. Basis for this amendment is found in the figures of the application.

AMENDMENTS TO CLAIM 11

Claim 11 has been amended to correct a typographical error by replacing "silicone" with, "silicon." Claim 11 has also been amended to more specifically require that the third insulating

layer must be located directly on the tunnel oxide layer, the select gate and the floating gate. Basis for this amendment is found in the figures of the application.

REJECTION UNDER 35 USC § 102

The Examiner has rejected claims 11-15 of the above-identified application under 35 U.S.C. § 102(e) as being clearly anticipated by U.S. Patent 6,245,614 (hereinafter "Hsieh"). After carefully reviewing Hsieh, the Applicant respectfully submits that the present invention is not described in Hsieh.

Hsieh discloses an EEPROM device comprising a silicon substrate (102), a gate oxide layer (105) formed over the silicon substrate (102), a select gate (112, 114, 116, 118) disposed on the gate oxide layer (105), a polysilicon spacer (126) formed on the wall of the select gate, a silicon oxide layer (138) formed between the select gate (112, 114, 116, 118) and an insulating layer (142) formed over the silicon oxide layer (138), the dielectric layer (108) and the polysilicon spacers (126) (See column 4, lines 55-58 of Hsieh). The device of Hsieh also includes a control gate (145) disposed on the insulating layer (142).

In the present invention, as claimed in claims 11-16, as amended, the structure of an EEPROM comprises a silicon substrate, a tunnel oxide layer, a select gate disposed over the tunnel oxide layer, a single floating gate aligned to one side of the select gate, a third insulating material located directly on the tunnel oxide layer, the select gate and the floating gate, and a control gate formed on the third insulating material. It is thus clear that the third insulating layer of the present invention is located directly on different elements of the EEPROM than the corresponding insulating layer (142) of Hsieh. Specifically, the insulating layer (142) of Hsieh is not located directly on the gate oxide layer (105) or the select gate (112, 114, 116, 118), and thus does not anticipate claim 11 of the present application since claim 11 requires that the third insulating layer be located directly on the tunnel oxide layer and the select gate. Accordingly, the structure of device of claim 11 of the present application is clearly novel over the structure of Hsieh.

Although the device of the present invention and the device of Hsieh each achieve a relatively large contact area between the floating gate and the control gate to obtain a higher capacitance and decrease the coupling ratio of the flash memory, they use different ways to achieve this goal. Because the third insulated material of the present invention is located directly

on the tunnel oxide layer, the select gate and the floating gate, and the floating gate is aligned to one side of the select gate, the floating gate of the present invention exposes the surface area from the top to the bottom of the outer side of the floating gate, relative to the position of the select gate, for contact with the control gate. In contrast, the floating gate (126) of Hsieh only exposes the upper area of the floating gate (126) to contact with the control gate (145) as a result of the insulating layer (142) being formed on the silicon oxide layer (138), the dielectric layer (108) and the polysilicon spacer (126), rather than directly on the tunnel oxide layer and select gate as in the present invention.

In addition, the device of Hsieh suffers from the disadvantage that to provide the structure of the device of Hsieh, it is necessary to deposit a silicon dioxide layer and subsequently etch the silicon dioxide layer and the dielectric layer to a predetermined thickness. See e.g. claim 1 and column 4, lines 51-58 of Hsieh. In contrast, the device of the present invention can be provided with a capacitance between the floating gate and the control gate comparable to that of the device of Hsieh, without the necessity to process a deposited layer using a costly etching step. Therefore, the device of the present invention has the additional advantage that it can provide cost savings in the fabrication of the device, relative to the fabrication process required to produce the device of Hsieh.

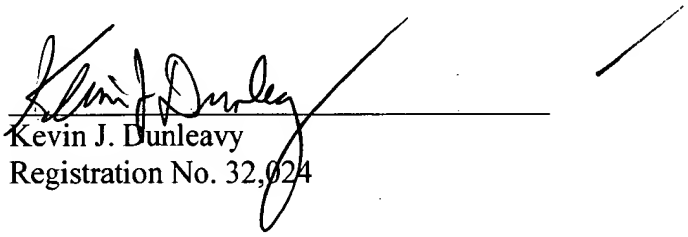
Finally, Hsieh considers it necessary to interpose a silicon oxide layer (138) between the gate oxide layer (105) and the insulating layer (142), and Hsieh considers it necessary to interpose a dielectric layer (108) between the select gate (112, 114, 116, 118) and the insulating layer (142). The skilled person would have no reason or motivation to leave out the silicon oxide layer (138) or the dielectric layer (108) of Hsieh and thus, it would not be obvious to modify the device of Hsieh to provide a third insulating layer located directly on the tunnel oxide layer and the select gate, as claimed in claim 11 of the present application. Therefore, the present invention, as claimed in claim 11, is also considered to be unobvious of Hsieh for at least this reason, as well as on the basis of the two advantages of the present invention discussed above, i.e. the larger contact area between the floating gate and the control gate, and the less costly fabrication process required to make the device of the present invention.

Claims 12-15 all depend from claim 11 and thus are considered to be patentable over Hsieh for at least the same reasons as are given for claim 11 in the above discussion. Claim 16 contains the same limitations as claim 11 that distinguish claim 11 over Hsieh as discussed above and thus

claim 16 is also considered to be patentable over Hsieh for the reasons given above with respect to claim 11.

Favorable consideration, withdrawal of the rejection of claims 11-15 under 35 U.S.C. §102(e) as anticipated by Hsieh, and issuance of a Notice of Allowance are requested.

Respectfully submitted,



Kevin J. Dunleavy
Registration No. 32,024

Customer No. 21302
KNOBLE & YOSHIDA
Eight Penn Center
Suite 1350
1628 John F. Kennedy Blvd.
Philadelphia, PA 19103
Telephone: (215) 599-0600
Facsimile: (215) 599-0601
Email: KJDunleavy@patentwise.com

Redline Version of Claim 11 Showing Amendments

11. (Twice Amended) A structure of an Electrically Erasable Programmable Read-Only Memory (EEPROM), comprising:

a silicon oxide substrate having a source/drain region,

a tunnel oxide layer disposed over said ~~silicone~~ silicon substrate;

a select gate disposed over said tunnel oxide layer, wherein said select gate is defined by a conductive layer covered with a first insulated material thereon and comprises a sidewall made of a second insulated material;

a sidewall forming a single floating gate aligned to one side of said select gate;

a third insulated material ~~disposed over~~located directly on said tunnel oxide layer, said select gate and said floating gate; and

a control gate formed on said third insulated material.

Redline Version of Proposed New Claim 12 Added by the Preliminary Amendment Dated March 18, 2003, Showing Amendments

~~12~~16. (Amended) A structure of an Electrically Erasable Programmable Read-Only Memory (EEPROM), comprising:

a silicon substrate having a source/drain region,

a tunnel oxide layer disposed over said ~~silicone~~silicon substrate;

a select gate disposed over said tunnel oxide layer, wherein said select gate is defined by a conductive layer covered with a first insulated material thereon and comprises a sidewall made of a second insulated material;

a floating gate aligned to one side of said select gate;

a third insulated material ~~disposed over~~located directly on said tunnel oxide layer, said select gate and said floating gate; and

a control gate formed on said third insulated material, ~~said control gate partially covers said third insulating material.~~ wherein said control gate partially covers said third insulating material.